SPECIFICATIONS FOR OLED MODULE

MODEL NO.
BL25664D-ERNNH$
VER.02

RoHS COMPLIANT

FOR MESSRS:

_____

ON DATE OF:

_____

APPROVED BY:

_____

BOLYMIN, INC.
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History of Vers ion

Version	Contents	Date	Note
01	NEW VERSION	2019/10/2	SPEC.
02	Coding system modify	2019/10/30	Page 4~5

C O N T E N T S

1. Numbering System

B	L	25664	D	-	E	R	N	N	H		$	
0	1	2	3		4	5	6	7	8	9	10	11

0	Bolymin	B			
1	Module Type	C	Character type	P	TAB /TCP type
		F	COF type	R	Color STN
		G	Graphic type	L	OLED
		O	COG type	Z	Customize
2	Format	2004	20 character type,4lines		
		12232	122 × 32 dots		
3	Version No.	D			
		-			
4	LCD Color	B	STN / Blue, OLED/Blue	H	HTN
		C	Color	T	TN
		F	FSTN	Y	STN/Yellow-green
		G	STN/Grey	D	OLED/Blue+Yellow
		A	OLED/Blue+Yellow+Green	E	OLED/Yellow
		L	OLED/Green	R	OLED/RED
		W	OLED/White	J	ASTN
		K	DFSTN	V	VA LCD
5	LCD Type	R	Positive/reflective	M	Positive/ transmissive
		P	Positive/transflective	N	Negative/ transmissive
		T	Negative/ transflective		
6	Backlight type/color	L	(LED)Array/yellow-green	G	(LED)Edge/yellow-green
		M	(LED)Array/amber	H	(LED)Edge/white
		R	(LED)Array/red	D	(LED)Edge/blue
		U	(LED)Array/blue	E	(EL)white
		W	(LED)Array/white	B	(EL)blue
		C	(CCFL) white	F	(LED)Array/RGB
		Y	(LED)Array/yellow	N	No backlight
		O	(LED)Array/orange	K	(LED)Edge/green
		A	(LED)Edge/amber	Q	(LED)Edge/red
		J	(LED)Array/green	I	(LED)Edge/RGB
		Z	(LED) arrayred/green	P	(LED)Edge/orange

		S	(LED)edge/RGW	T	(LED)edge red/green
		V	EL blue/green`	X	(LED) Edgewhite /red
7	CGRAM Font	J	English/Japanese Font	C	English/Cyrillic Font
		G	Chinese(simple)	H	English/Hebrew Font
		E	English/European Font (ST7066U0B-BB)	S	English/European Font (ST7066U-0E-BB)
		F	Chinese(traditional)	M	Japanese-Kanji
		Z	Z=Chinese(simple)+Chinese (traditional)+Japanese+Korean	K	Korean (only for BG16032A BG24064C)
		A	English/Arabic Font	D	Chinese (simple/traditional) English/Japanese
		B	English/Japanese/European	N	None
8	View Angle /Operation Temperature	B	Bottom/Normal Temperature06:00	W	Top/Wide Temperature 12:00
		H	Bottom/Wide Temperature 06:00	E	Top/Ultra Temperature 12:00
		C	9H/Normal Temperature 09:00	U	Bottom/Ultra wide Temperature 06:00
		T	Top/Normal Temperature 12:00	F	9H/Ultra wide Temperature 09:00
		G	3H/Wide Temperature 3:00	D	9H/Wide Temperature 09:00
		I	3H/ Ultra Wide Temperature 3:00		
9	Special Code	N	Positive voltage for LCD	T	Negative voltage and Temperature compensation for LCD
		P	Touch panel	3/5	3/5 voltage logic power supply
10	RoHS	$			
11	Customer Code	00 0 ~ 99 0 、AA 0 ~ ZZ 0			

2.General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of dots	256×64	dots
Module dimension (L*W*H)	146.0 x 65.0 x 2.0	mm
View area	137.65 x 35.89	mm
Active area	135.65 x 33.89	mm
Dot size	0.5 x 0.5	mm
Dot pitch	0.53 x 0.53	mm

(2) Controller IC: SSD1322 Controller

(3) Temperature Range

Operating	-40 ~ +70℃
Storage	-40 ~ +85℃

3.Absolute Maximum Ratings

Item	Symbol	Condition	Min	Max	Unit
Operating Temperature	TOP		-40	+70	℃
Storage Temperature	TST		-40	+85	℃
Supply Voltage for Operation	V_{CI}		-0.3	4.0	V
Supply Voltage for Logic	VDD		-0.5	2.75	V
Supply Voltage for I/O Pins	VDDIO		-0.5	V_{CI}	V
Supply Voltage for Display	VCC		-0.5	16.0	V
Operating life time		60cd/m², 50% checkerboard	100000		Hrs
Operating life time		40cd/m², 50% checkerboard	150000		Hrs

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The define temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80℃.

Note 4: V_{CC} = 15.0V, T a = 25℃, 50% Checkerboard. Software co nfiguration follows initialization. End of lifetime is specified as 50% of initial brightness reached. Theaverage operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

Note5: Lifetime should be counted once shipping out from our warehouse . But the exact lifetime must depend on customer's operation environment and application.

4.Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage for Operation	V_{CI}		2.4	2.8	3.5	
Supply Voltage for Logic	V_{DD}	—	2.4	2.5	2.6	V
Supply Voltage for I/O Pins	V_{DDIO}		1.65	1.8	V_{CI}	
Supply Voltage for Display (Supplied Externally)	V_{cc}	Note 6	14.5	15.0	15.5	V
Input High Vol	V_{IH}	—	$0.8V_{DD}$	—	V_{DD}	V
Input Low Vol	V_{IL}	—	—	—	$0.2V_{DD}$	V
Operating Current for V_{CC} (V_{CC} Supplied Externally)	I_{CC}	Note 7	—	64	80	m A

Note 6: Brightness (L br) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 7: V_{CI} = 2.8V, V_{CC} = 15V, 100% Display Area Turn on.

5.Optical Characteristics

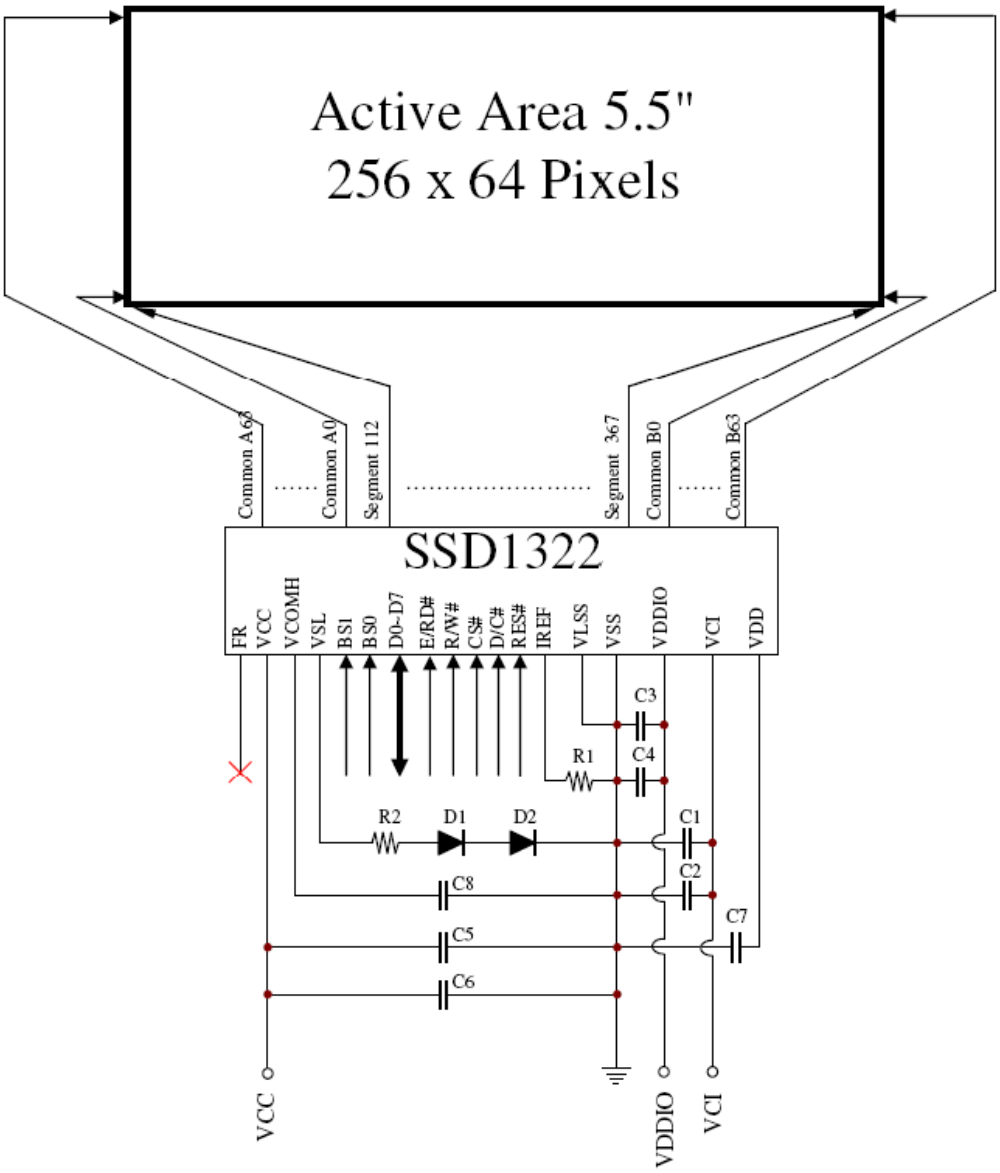
Item	Min.	Typ.	Max.	Unit
View Angle	—	Free	—	deg
Dark Room contrast	—	>10,000:1	—	—
Pixel Luminance	40	60		cd/m2
CIE x (Yellow)	0.46	0.50	0.54	
CIE y (Yellow)	0.45	0.49	0.53	

6.Interface Pin Function

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4">Power Supply</td></tr>
<tr><td>26</td><td>VCI</td><td>P</td><td>Power Supplly for Operatiion
This is a voltage supply pin. It must be connected to external source & should be equal to or higher than V_{DD}& V_{DDIO}.</td></tr>
<tr><td>25</td><td>VDD</td><td>P</td><td>Power Supplly for Core Logiic Ciircuiit
This is a voltage supply pin. It can be supplied externally (within the range of 2.4~2.6V) or regulated internally from V_{CI}.
A capacitor should be connected between this pin & V_{SS} under all circumstances.</td></tr>
<tr><td>24</td><td>VDDIO</td><td>P</td><td>Power Supplly for I/O Piin
This pin is a power supply pin of I/O buffer. It should be connected to VCI or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals…) pull high, they should be connected to VDDIO.</td></tr>
<tr><td>2</td><td>VSS</td><td>P</td><td>Ground of Logiic Ciircuiit
This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>3,29</td><td>VCC</td><td>P</td><td>Power Supplly for OEL Panell
These are the most positive voltage supply pin of the chip. They must be connected to external source.</td></tr>
<tr><td>5,28</td><td>VLSS</td><td>P</td><td>Ground of Anallog Ciircuiit
These are the analog ground pins. They should be connected to VSS externally.</td></tr>
<tr><td colspan="4">Driver</td></tr>
<tr><td>22</td><td>IREF</td><td>I</td><td>Current Reference for Briightness Adjjustment
This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10μA maximum.</td></tr>
<tr><td>4</td><td>VCOMH</td><td>P</td><td>Volltage Output Hiigh Levell for COM Siignall
This pin is the input pin for the voltage output high level for COM signals.
A tantalum capacitor should be connected between this pin and VSS.</td></tr>
<tr><td>27</td><td>VSL</td><td>P</td><td>Volltage Output Low Levell for SEG Siignall
This is segment voltage reference pin.
When external VSL is not used, this pin should be left open.
When external VSL is used, this pin should connect with resistor and diode to ground.</td></tr>
<tr><td colspan="4">Testing Pads</td></tr>
<tr><td>21</td><td>FR</td><td>O</td><td>Frame Frequency Triiggeriing Siignall
This pin will send out a signal that could be used to identify the driver status.Nothing should be connected to this pin. It should be left open individually.</td></tr>
<tr><td colspan="4">Interface</td></tr>
<tr><td>16
17</td><td>BS0
BS1</td><td>I</td><td>Communiicatiing Protocoll Sellect
These pins are MCU interface selection input. See the following table:
<table>
<tr><td></td><td>BS0</td><td>BS1</td></tr>
<tr><td>3-wire Serial</td><td>1</td><td>0</td></tr>
<tr><td>4-wire Serial</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>1</td><td>1</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>0</td><td>1</td></tr>
</table></td></tr>
<tr><td>20</td><td>RES#</td><td>I</td><td>Power Reset for Controllller and Driiver
This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.</td></tr>
<tr><td>19</td><td>CS#</td><td>I</td><td>Chiip Sellect
This pin is the chip select input.
The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
</table>

Pin Number	Symbol	I/O	Function
18	D/C#	I	**Data/Command Controll** This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. When 3-wire serial mode is selected, this pin must be connected to VSS. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
14	E/RD#	I	**Read/Wriite Enablle or Read** This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial mode is selected, this pin must be connected to V_{SS}.
15	R/W#	I	**Read/Wriite Sellect or Wriite** This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.
6~13	D7~D0	I/O	**Host Data Input/Output Bus** These pins are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. Unused pins must be connected to VSS except for D2 in serial mode.
Reserve			
23	N.C.	-	**Reserved Piin** The N.C. pin between function pins is reserved for compatible and flexible design.
1,30	N.C. (GND)		**Reserved Piin (Supportiing Piin)** The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.

7.Block Diagram



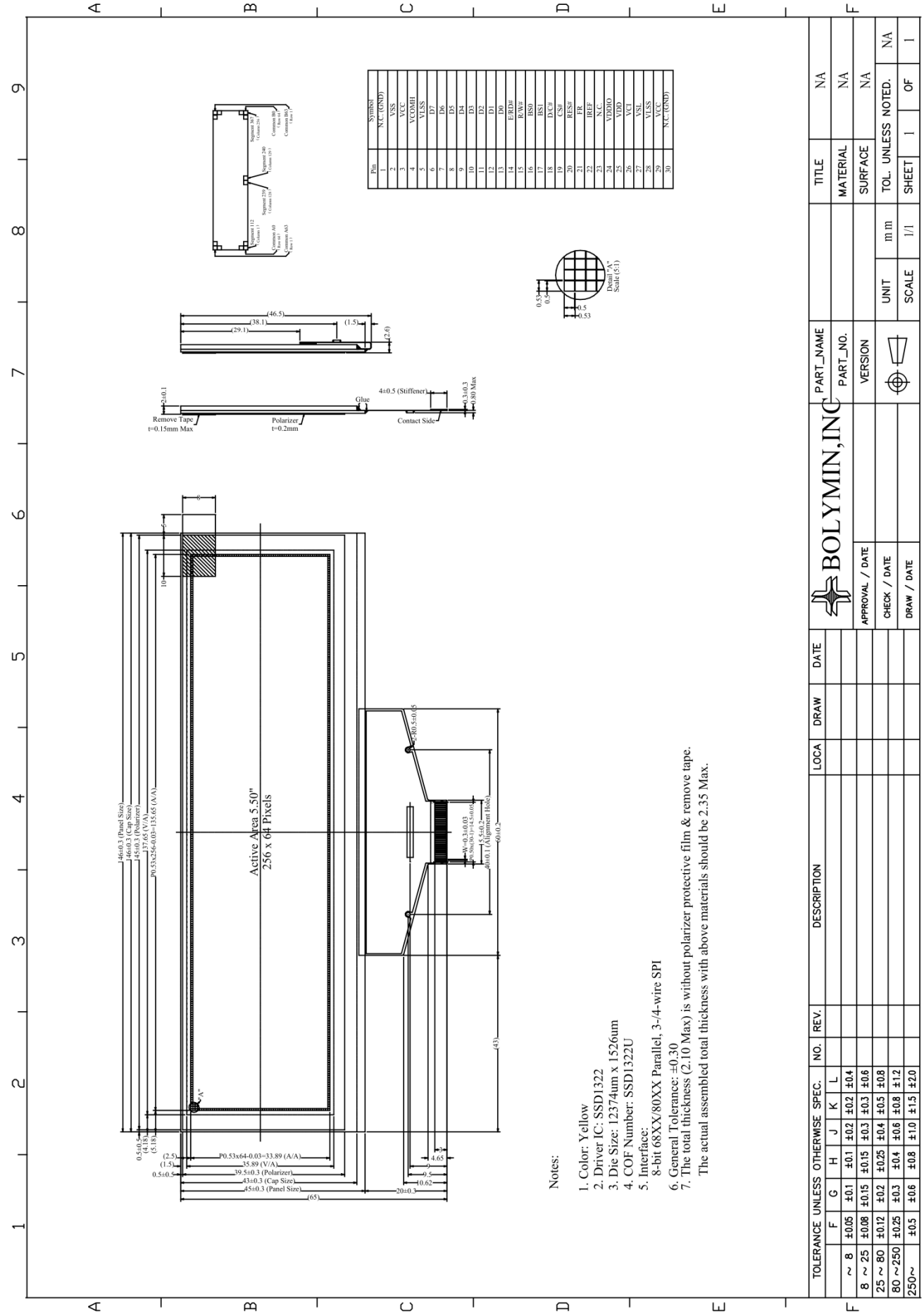
C1, C3, C5 :0.1 μF
C2, C4 :4.7 μF
C6 :20 μF
C7 :1 μF
C8 :4.7 μF / 25V Tantalum Capacitor
R1 :910kΩ, R1 = (Voltage at IREF - VSS) / IREF
R2 :50Ω, 1/4W
D1, D2 :0.7V, 0.5W

MCU Interface Selection : Base on BS0 and BS1 connection
Pins connected to MCU interface : D7~D0, E/RD#, R/W#, D/C#, CS#, and RES#
Showed as below table :

BS1	BS0	Interface mode	Data bus								Control bus				
			D7	D6	D5	D4	D3	D2	D1	D0	CS#	D/C#	R/W#	E/RD#	RES#
0	0	4-wire SPI	**0**	**0**	**0**	**0**	**0**	**NC**	SDIN	SCLK	CS#	D/C#	**0**	**0**	RES#
0	1	3-wire SPI	**0**	**0**	**0**	**0**	**0**	**NC**	SDIN	SCLK	CS#	**0**	**0**	**0**	RES#
1	0	8bit 8080	D7	D6	D5	D4	D3	D2	D1	D0	CS#	D/C#	R/W#	E	RES#
1	1	8bit 6800	D7	D6	D5	D4	D3	D2	D1	D0	CS#	D/C#	WR#	RD#	RES#

Note :
a. " 0 " is connected to VSS.
b. " 1 " is connected to VDD.
c. " NC " is non-connected.

8.Drawing



Notes:

1. Color: Yellow
2. Driver IC: SSD1322
3. Die Size: 12374um x 1526um
4. COF Number: SSD1322U
5. Interface:
   8-bit 68XX/80XX Parallel, 3-/4-wire SPI
6. General Tolerance: ±0.30
7. The total thickness (2.10 Max) is without polarizer protective film & remove tape.
   The actual assembled total thickness with above materials should be 2.35 Max.

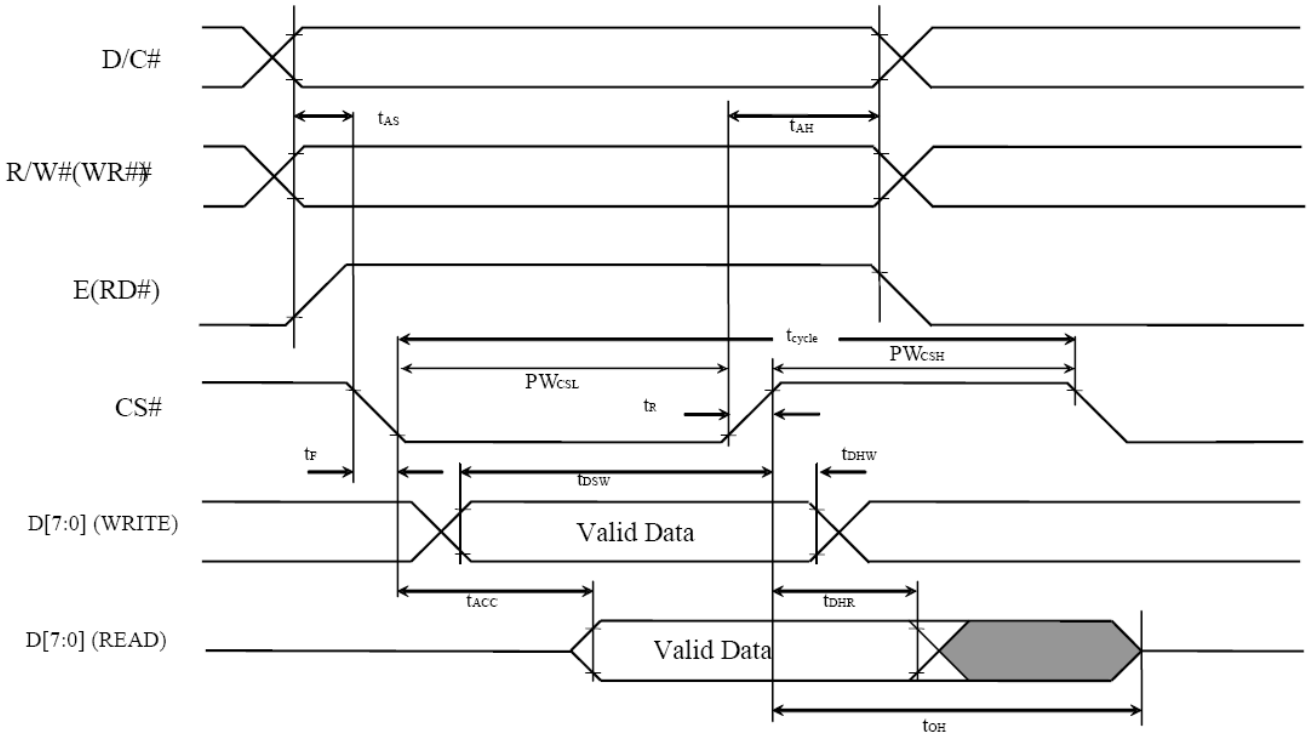
9.SSD1322controller data

9.1 Timing Characteristics

68XX-Series MPU Parallel Interface Timing Characteristics

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300		ns
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	0		ns
t_{DSW}	Write Data Setup Time	40		ns
t_{DHW}	Write Data Hold Time	7		ns
t_{DHR}	Read Data Hold Time	20		ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120		ns
	Chip Select Low Pulse Width (Write)	60		ns
PW_{CSH}	Chip Select High Pulse Width (Read)	60		ns
	Chip Select High Pulse Width (Write)	-		ns
t_R	Rise Time	-		ns
t_F	Fall Time			

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.65V, V_{CI} = 3.3V, T_a = 25℃)

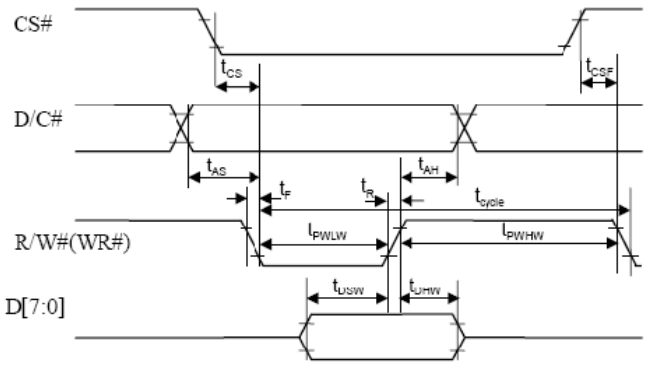


80XX-Series MPU Parallel Interface Timing Characteristics:

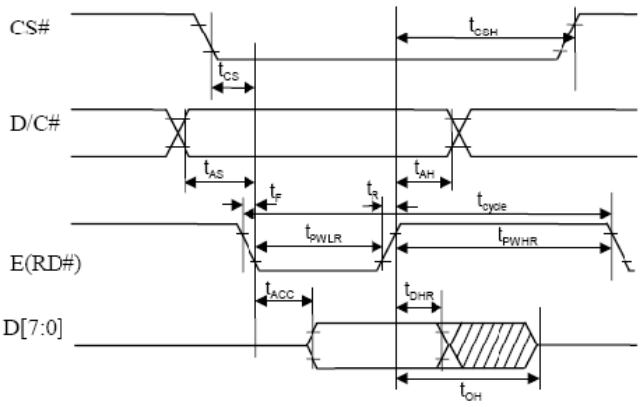
Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	-	ns
t_F	Fall Time	-	-	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.65V, V_{CI} = 3.3V, T_a = 25℃)

Write cycle



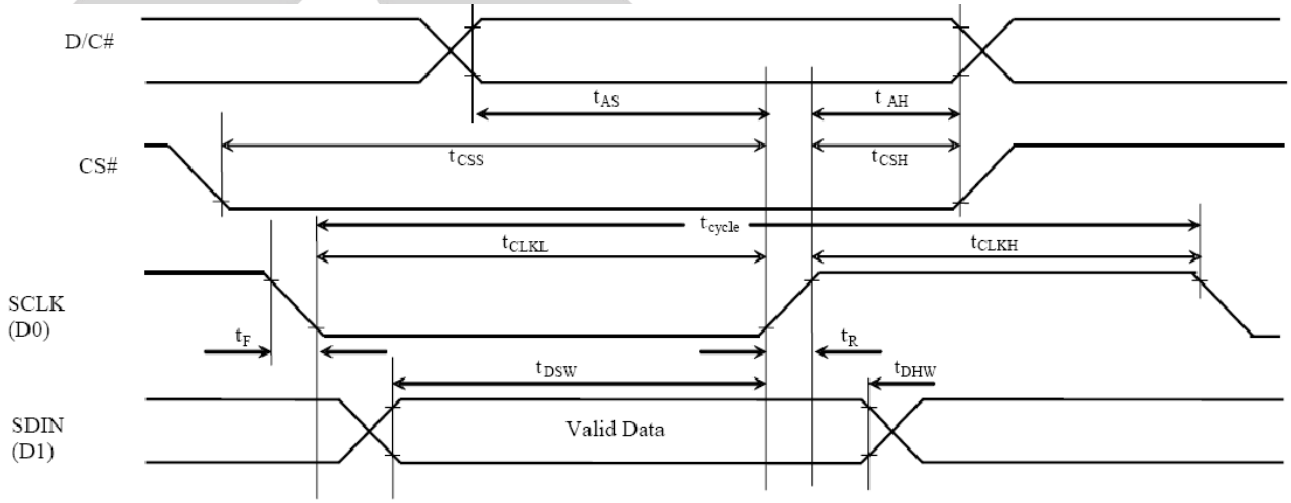
Read cycle

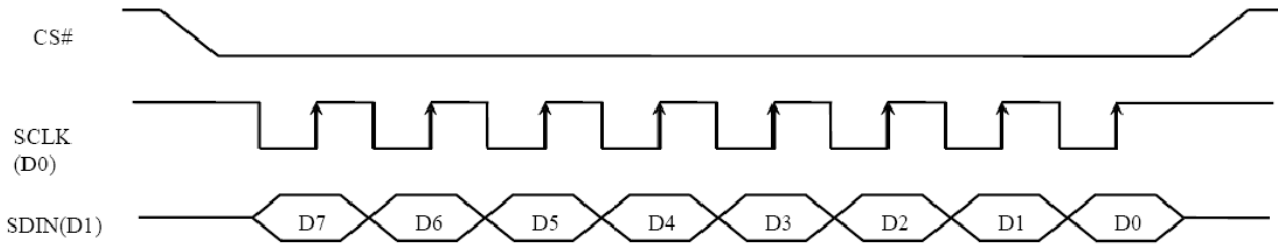


Serial Interface Timing Characteristics: (4-wire serial)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.65V, V_{CI} = 3.3V, T_a = 25℃)

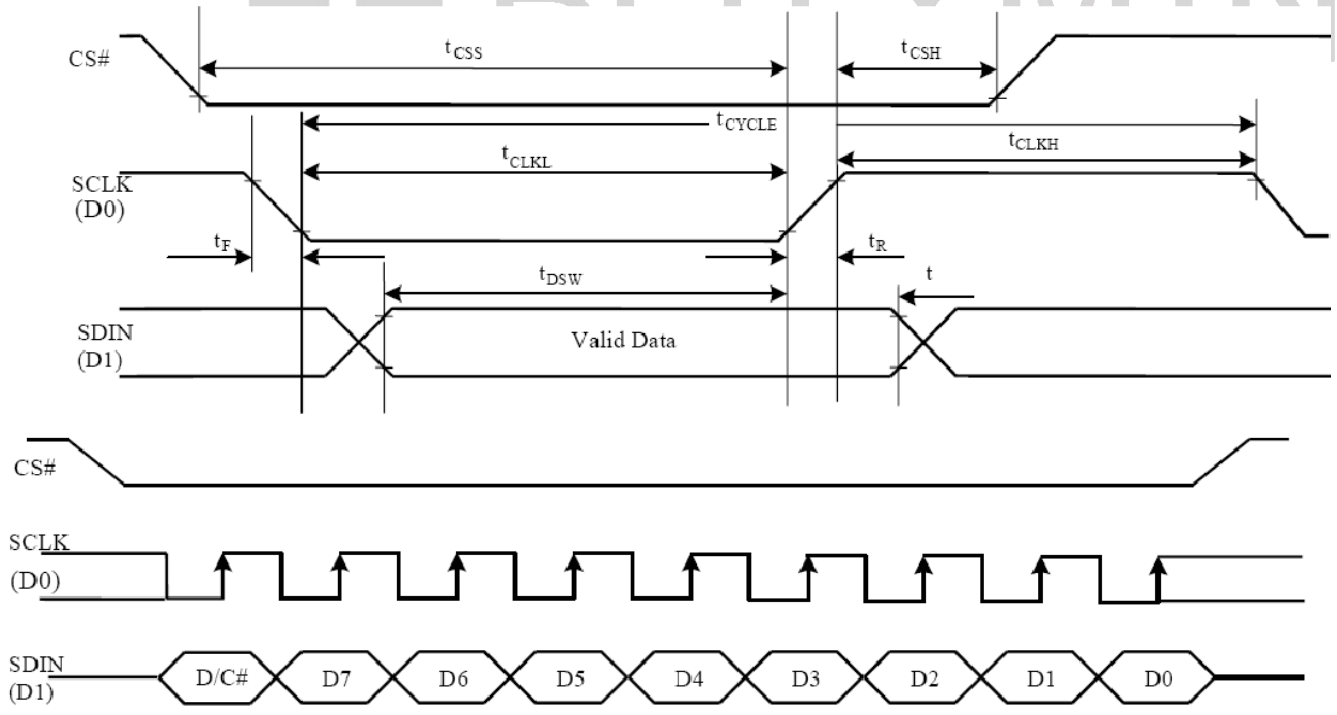




Serial Interface Timing Characteristics: (3-wire Serial)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.65V, V_{CI} = 3.3V, T_a = 25℃)



9.2Display Control Instruction

Command tablerefer to IC spec.:SSD1322

10.Quality Assurance

10.1 **Inspection conditions**

1. The inspection and meaurement are performed under the following conditions,
2. unless otherwise specified.
3. Temperature: 25±5℃
4. Humidity: 50±10%R.H.
5. Distance between the panel and eyes of the inspector≧30cm

10.2 **Inspection Parameters**

Severity	Inspection Item	Defect	Remark
Major Defect	1. Panel	(1) Non-displaying	
		(2) Line defects	
		(3) Malfunction	
		(4) Glass cracked	
	2. Film	(1) Film dimension out of specification	Can not be assembled
	3. Dimension	(1) Outline dimension out of specification	
Minor Defect	1. Panel	(1) Glass scratch	Appearance defect
		(2) Glass cutting NG	
		(3) Glass chip	
	2. Polarizer	(1) Polarizer scratch	
		(2) Stains on surface	
		(3) Polarizer bubbles	
	3. Displaying	(1) Dim spot、Bright spot、dust	
	4. Film	(1) Damage (2) Foreign material	

<table>
<tr><th>Description</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>1. Glass scratch</td><td>
<table>
<tr><th>Width (mm)
W</th><th>Length (mm)
L</th><th>number of pieces permitted</th></tr>
<tr><td>W≦0.03</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td>0.03＜ W≦0.05</td><td>L≦3</td><td>3</td></tr>
<tr><td>0.05＜ W</td><td>------</td><td>None</td></tr>
<tr><td>beyond A.A.</td><td>------</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>2. Polarizer bubble</td><td>
<table>
<tr><th>Size</th><th>number of pieces permitted</th></tr>
<tr><td>Φ≦0.2</td><td>Ignore</td></tr>
<tr><td>0.2＜Φ≦0.5</td><td>2</td></tr>
<tr><td>0.5＜Φ</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>3. Dimming spot、
Lighting spot、
Dust</td><td>
<table>
<tr><th>average</th><th>number of</th></tr>
<tr><td>D ≦0.1</td><td>Ignore</td></tr>
<tr><td>0.1＜ D ≦0.15</td><td>2</td></tr>
<tr><td>0.15＜ D ≦0.2</td><td>1</td></tr>
<tr><td>0.2 ＜ D</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
D=(long diameter + short diameter)/2.
Pixel off is not allowed.
</td><td>Minor</td></tr>
</table>

10.3 WARRANTY POLICY

Bolymin . Will provide one-year warranty for the products only if under specification operating conditions.
If there are functional defects found during the period of warranty, the defective products would be replaced on a one-to-one basis.
Bolymin would not be responsible for any direct/indirect liabilities consequential to any parties.

10.4 MTBF

10.4.1 .MTBF based on specific test condition is 30K hours.

10.4.2 Test Condition:

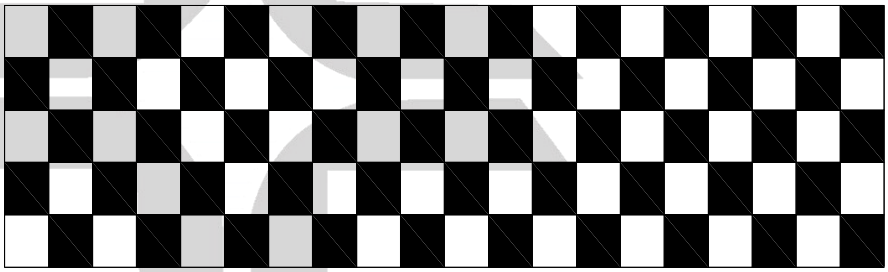
10.4.2.1 Supply Voltage: Vcc=15V

10.4.2.2 Luminance: <80 cd/m^2

10.4.2.3 Operation temperature and humidity:<25 ℃ and 50%RH

10.4.2.4 Run-Patterns

:



10.4.3 Test Criteria:

Luminace has decayed to less than 50% of the initial measured luminance.

11.Reliability

■Content of Reliability Test

NO.	Items.	Specification	Applicable Standard
1	High temp. (Non-operation)	85℃, 240hrs	——
2	High temp. (Operation)	70℃, 120hrs	——
3	Low temp. (Operation)	-40℃, 120hrs	——
4	High temp. / High. humidity (Operation)	60℃, 90%RH, 120hrs	——
5	Thermal shock(Non-operation)	-40℃ ~85℃ (-40℃ /30min; transit /3min; 85℃ /30min; transit /3min) 1cycle: 66min, 100 cycles.	——
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	——

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1 & 4 & 5.

Criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: >50% of initial value.
4. Current consumption : within ±50% of initial value.

Reliability Test

Bolymin only guarantees the reliability of the panel under the test conditions and durations listed in the specification, and is not responsible for any test results that are conducted using more stringent conditions and/or with lengthened durations. Also, when the testing the panel in a chamber or oven, make sure they won't produce any condensation on the panel, especially on the electrical leads, before lighting on the panel to see if it passes the test. Also the panel should rest for about an hour at room temperature and pressure before the measurement, as indicated in the specification. Be aware that one should use fresh panel for each of the reliability test items listed in the specification, in other words, don't use the panels that were tested for subsequent tests.

12. Precautions for Handling

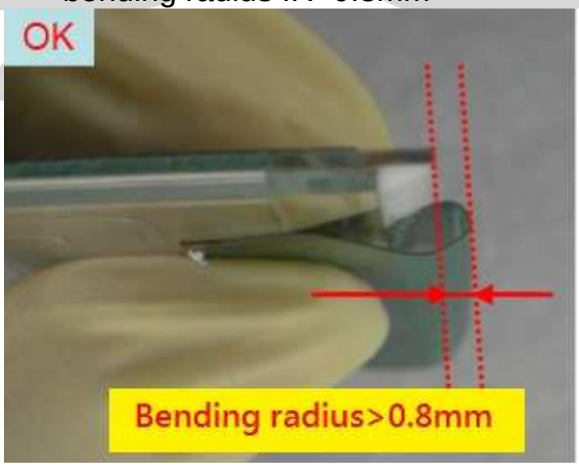
12.1 When handling the module, wear powder-free antistatic rubber finger cots, and be careful not to bend and twist it.

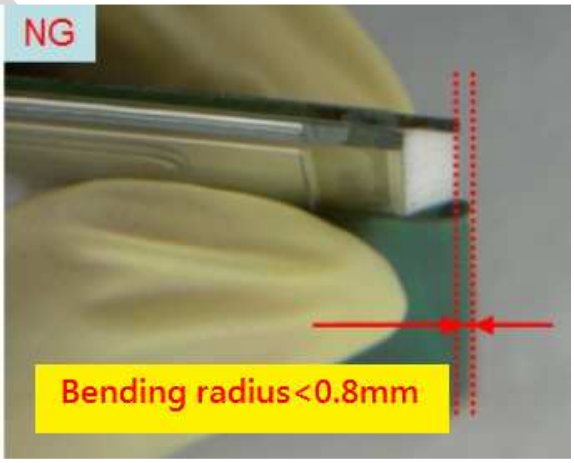
12.2 The OLED module is consisted of glass and film, and it should avoid pressure, strong impact, orbeing dropped from a height.

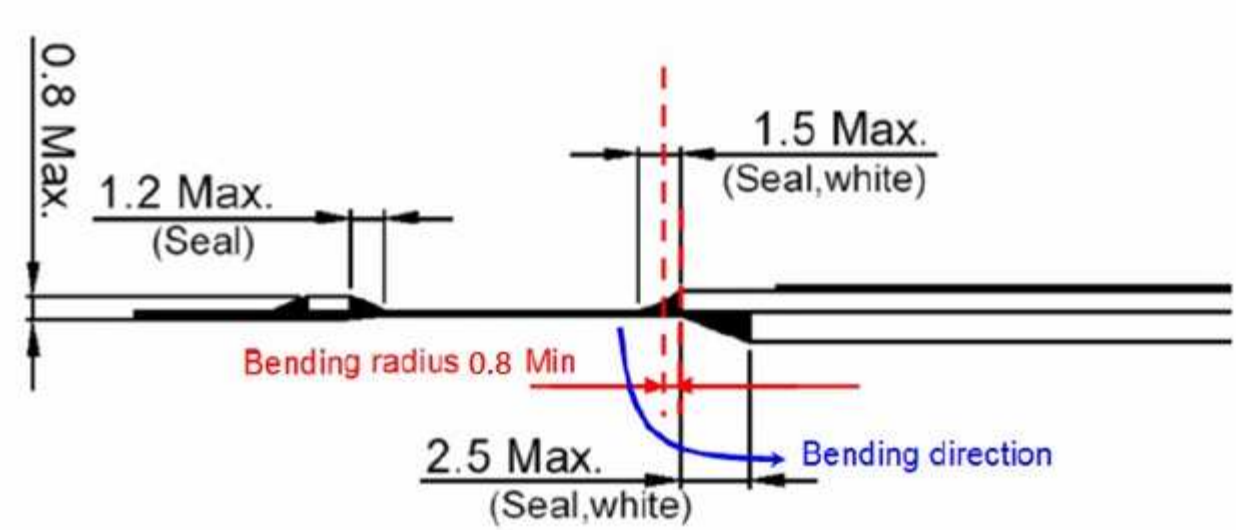
12.3 The OLED module is an electronic component and is subject to damage caused by Electro Static

Discharge (ESD) and hence normal ESD precautions must be taken when handling it. Also, appropriate ESD protective environment must be administered and maintained in the production line. When handling and assembling the panel, wear an antistatic wrist strap with the alligator clip attached to the ground to prevent ESD damage on the panel. Also, ground the tools being used for panel assembly and make sure the working environment is not too dry to cause ESD problems. (See the photos below).

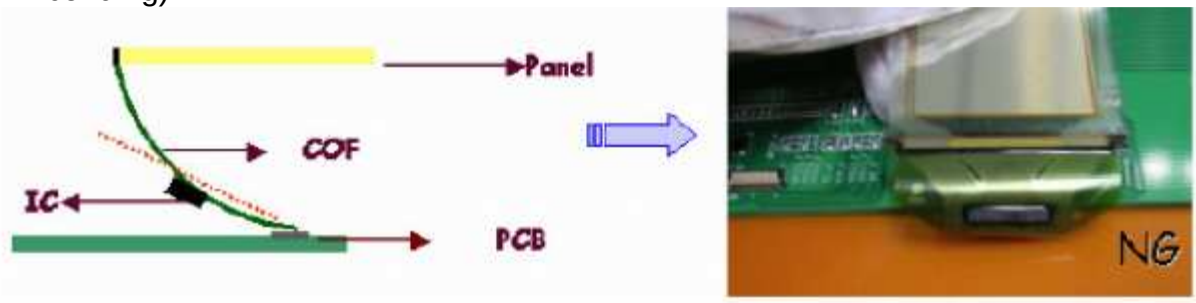
12.4 Please do not bend the film near the substrate glass.(this could cause film peeling and COF damage) and the peeling strength about 600g/cm, the bending <20times and the bending radius :R>0.8mm



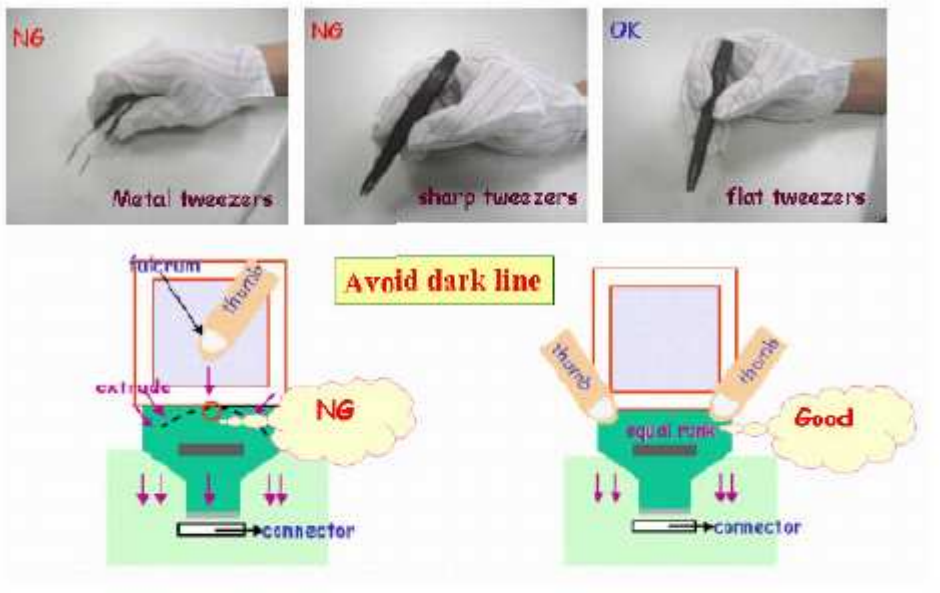




12.5 Avoid bending the film at IC bonding area.(>1.5mm)(this could damage the ILB bonding)



12.6 Use both thumbs to insert COF into the connector when assembling the panel. See the photo on the far right below for correct insertion of the film into the connector (one-handed insertion exerts uneven force on the film and could cause its breakage, photo on the left)



12.7 Do not wipe the pin of film with the dry or hard materials that will damage the surface. When cleaning the display surface, use soft cloth solvent and wipe gently (Recommend solvent: IPA, alcohol), and do not wipe the display with dry or hard materials that will damage the polarizer surface and do not use the solvent like: Water, Acetone, Aromatic

13. Precautions for Electrical

13.1. Design using the settings in the specification

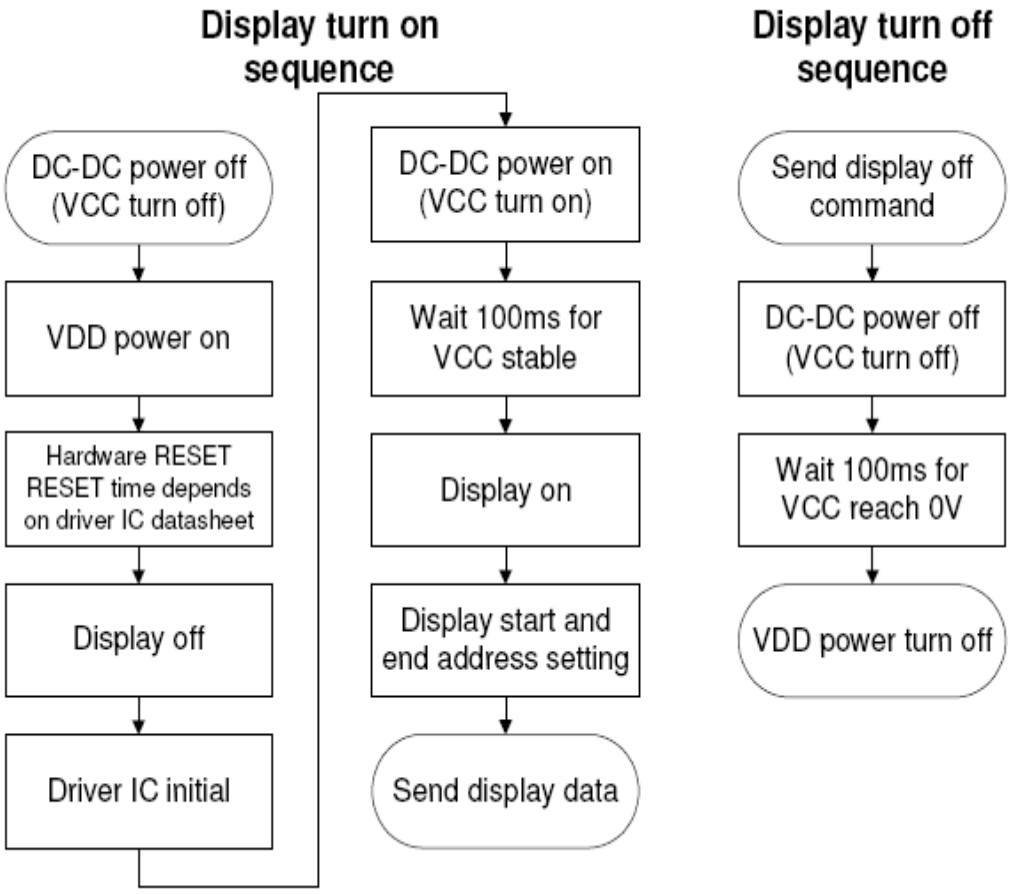
It is extremely important to design and operate the panel using the settings listed in the specification. This includes voltage, current, frame rate, duty cycle... etc. Operation of the OLED outside the specified range in the specification should be entirely avoided to ensure proper operation of the OLED.

13.2. Maximum Ratings

To ensure proper operation of the panel, never design the panel with parameters running over the maximum ratings listed in the specification. Also the logic voltages such as VIL and VIH have to be within the specified range in the specification to prevent any improper operation of the panel.

13.3 Power on/off procedure

Any operation that does not comply with the procedure could cause permanent damage of the IC and should be avoided. When the logic power is not on, do not activate any input signal. Abrupt shutdown of power to the module, while the OLED panel is on, could cause OLED panel malfunctioning.



13.4 Power savings

To save power consumption of the OLED, one can use partial display or sleep mode when the panel is not fully activated. Also, if possible, make maximum use of black background to save power. The OLED is a self-luminous device, and a particular pixel cluster or image can be lit on via software control, so power savings can be achieved by partial display or dimming down the luminance. Depending on the application, the user can choose among Ultra Bright Mode, Normal Operation Mode, and Sleeping Mode.

The power consumption is almost in direct proportion to the brightness of the panel, and also in direct proportion to the number of pixels lit on the panel, so the customer can save the power by the use of black background and Sleeping Mode. One benefit from using these design schemes is the extension of the OLED lifetime.

13.5 Residual Image (Image Sticking)

The OLED is a self-emissive device. As with other self-emissive device or displays consisting of self-emissive pixels, when a static image frozen for a long period of time is changed to another one with all-pixels-on background, residual image or image sticking is noticed by the human eye. Image sticking is due to the luminance difference or contrast between the pixels that were previously turned on and the pixels that are newly turned on. The time when image sticking happens depends on the luminance decay curve of the display. The slower the decay, the less prominent the image sticking is. It is strongly recommended that the user employ the following three strategies to minimize image sticking

13.5.1 Employ image scrolling or animation to even out the lit-on time of each and every pixel on the display, also could use sleeping mode for reduced the residual image and extend the power capacity.

13.5.2 Minimize the use of all-pixels-on or full white background in their application because when the panel is turned on full white, the image sticking from previously shown patterns is the most revealing. Black background is the best for power savings, greatest visibility, eye appealing, and dazzling displays

13.5.3 If in the reliability test when a static logo is used, change the pattern into its inverse (i.e., turn off the while pixels and turn on the previously unlit pixels) and freeze the inverse pattern as long as the original logo is used, so every pixel on the panel can be lit on for about the same time to minimize image sticking, caused by the differential turn-on time between the original and its reverse patterns

14. Precautions for Storage

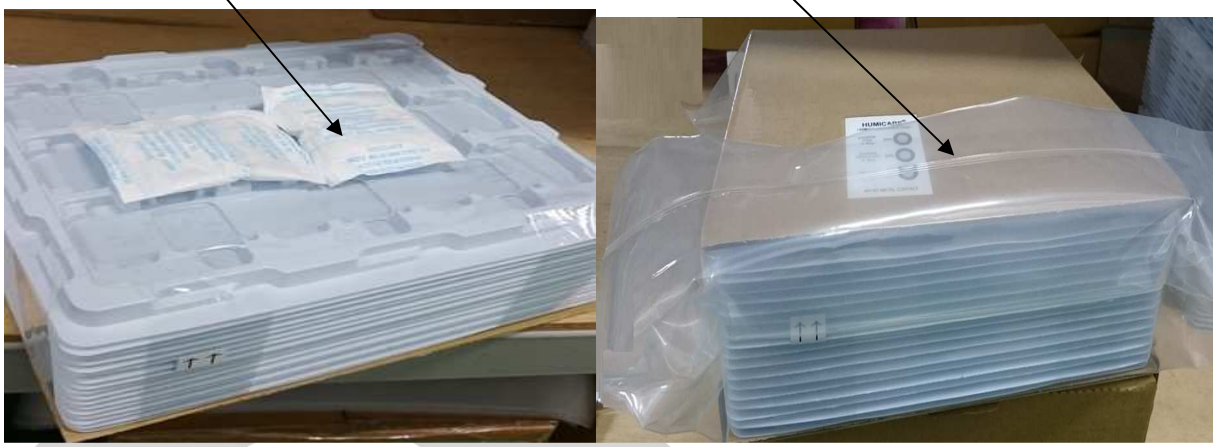
Although the storage conditions and guarantee period are indicated in the specification, it is advisable to store the packed cartons or packages at 23℃±5℃,55%±10%RH(Note A), Do not store the OLED module under direct sunlight or UV light and for best panel performance. The constant working OLED display module decays slower than the module that is not working. And it's better to use the module on the field within one month after unpacking the package.

Note (A):

Vacuum Packaging

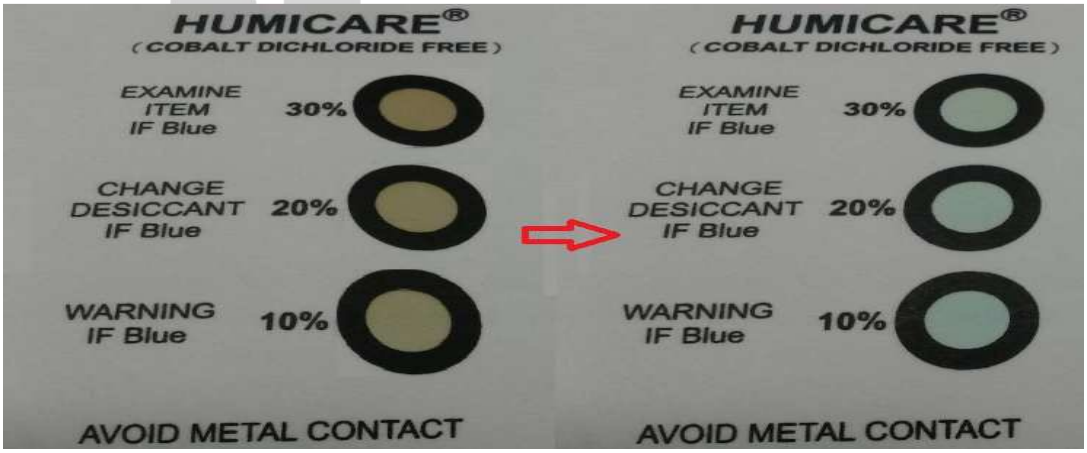
Desiccant x 2

Humidity indicator card



Humidity indicator card

As the humidity increases, the chemically impregnated spots change from a brown color (DRY) to a bluecolor (HUMID).



※The OLED module would be decayed due to humidity, please keep the environment dry whenever in the operating or storage.